Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)

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ABSTRACT
The theoretical lower limit of subthreshold swing in MOSFETs (60 mV/decade) significantly restricts low voltage operation since it results in a low ON to OFF current ratio at low supply voltages. This paper investigates extremely-low power circuits based on new Si/SiGe HEterojunction Tunneling Transistors (HETTs) that have subthreshold swing < 60 mV/decade. Device characteristics as determined through Technology Computer Aided Design (TCAD) tools are used to develop a Verilog-A device model to simulate and evaluate a range of HETT-based circuits. We show that a HETT-based ring oscillator (RO) shows a 9−19X reduction in dynamic power compared to a CMOS RO. We also explore two key differences between HETTs and traditional MOSFETs, namely asymmetric current flow and increased Miller capacitance, analyzing their effect on circuit behavior and proposing methods to address them. Finally, HETT characteristics have the most dramatic impact on SRAM operation and hence we propose a novel 7-transistor HETT-based SRAM cell topology to overcome, and take advantage of, the asymmetric current flow. This new HETT SRAM design achieves 7−37X reduction in leakage power compared to CMOS.

Categories and Subject Descriptors
B.3.1 [**Memory Structures**]: Semiconductor Memories – *Static Memory (SRAM)*; B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced Technologies, Memory Technologies, VLSI (very large scale integration)*; B.8.0 [**Performance and Reliability**]: General

General Terms: Performance, Design, Reliability

Keywords: Low Power Applications, Tunneling Transistor, SRAM Design

1. INTRODUCTION
Low voltage operation is one of the most effective low power design techniques due to its quadratic dynamic energy savings. Recently, a number of works [1-4] have shown aggressive supply voltage reduction to near or below the threshold voltage (V_{th}) of MOSFET devices with considerable reduction in power consumption. However, this power improvement has come at the cost of operation speed (typically <10 MHz). At such low supply voltages, ON current drops dramatically due to lack of gate overdrive resulting in large signal transition delays. To regain this performance loss it is possible to reduce the threshold voltage. However, this exponentially increases OFF current, which is particularly problematic in applications that spend significant time in standby mode [5]. For instance, lowering the supply voltage from 500mV to 250mV while enforcing iso-performance by reducing the V_{th} increases leakage power by 275X in a commercial bulk-CMOS 45nm technology, which is unacceptable.

To address this dilemma, there has been recent interest in new devices with significantly steeper subthreshold slopes than traditional MOSFETs [6-9]. A steep subthreshold slope enables operation with a much lower threshold voltage while maintaining low leakage. In turn, a low V_{th} enables low voltage operation while maintaining performance. Hence, steep subthreshold slopes can provide power efficient operation without loss of performance.

In this paper, we investigate circuit design using the recently proposed Si/SiGe HEterojunction Tunneling Transistor (HETT) [10]. The Si/SiGe heterostructure uses gate-controlled modulation of band-to-band tunneling to obtain subthreshold swings of less than 30 mV/decade with a large ON current of 0.42mA/μm at V_{ds} = 0.5V. Furthermore, Si/SiGe heterostructures are fully compatible with current MOSFET fabrication and can leverage the extensive prior investment in CMOS fabrication technology. Currently, several industry and university teams are actively developing Si/SiGe HETT type transistor structures, and initial devices have been experimentally demonstrated [11-12].

We explore the key differences between HETTs and traditional MOSFETs that must be considered in the design of circuits using these new devices. Most significantly, HETTs display asymmetric conductance. In MOSFETs, the source and drain are interchangeable, with the distinction only determined by the voltages during operation. However, in HETTs, the source and drain are determined at the time of fabrication, and the current flow for $V_{ds} < 0$ is substantially less than for $V_{ds} > 0$ (in an NHETT). Hence, HETTs can be thought to operate "uni-directionally", passing logic values only in one direction, which has significant implications on logic and especially SRAM design. Our analysis shows that another effect is a large increase in gate-to-drain capacitance (i.e., Miller capacitance) in HETTs compared to MOSFETs. This excess Miller capacitance can cause undesirable artifacts in the switching behavior of HETTs that is not present in MOSFETs. These differences in device operation and characteristics require careful study to understand their circuit design implications. In this paper, we show that HETT-based logic circuits are capable of improving energy efficiency by 19X compared to CMOS when operated at a supply voltage of 0.23 V. We particularly study SRAM design which is most impacted by the novel characteristics of HETTs. We show that the unidirectional characteristic of HETTs can actually be exploited in SRAM design to enable a novel 7T robust SRAM cell.

The remainder of this paper is organized as follows: First, we briefly discuss HETT device operation and highlight the differences between the physics of HETT and MOSFET operation. Second, we introduce our modeling method for HETTs to enable circuit simulation of these devices, and examine dynamic power reduction in standard circuits compared to a commercial bulk CMOS 45nm technology. Third, we discuss the impact of the unique characteristics of HETTs on circuit behavior and describe how to address these issues. Finally, we present the new HETT-based SRAM cell topology that takes advantage of the asymmetric current flow of HETTs and quantify robustness improvements and leakage power reductions compared with CMOS-based SRAM.

2. HETT DEVICE CHARACTERISTICS
The 60 mV/decade subthreshold slope limitation of conventional MOSFETs arises due to the thermionic nature of the turn-on mechanism. Tunneling transistors do not suffer from this fundamental limitation, since the turn-on in these devices is not governed by thermionic emission over a barrier.

ISLPED'09, August 19–21, 2009, San Francisco, California, USA.

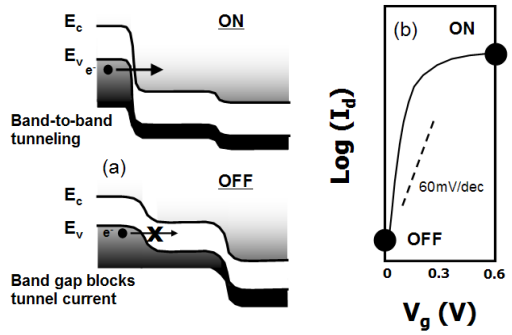


Figure 1. Tunneling FET device concept as depicted by a) band diagrams in the source-to-drain direction, and b) qualitative current-voltage characteristics.

Figure 1 illustrates the basic concept of tunneling transistor operation. In an n-type tunneling transistor, the source is doped p-type, the channel is undoped or lightly doped, and the drain is n-type. As shown in Figure 1, when the gate is biased positively the device is turned on because electrons in the valence band of the p-type source can tunnel into the conduction band of the channel. If the Fermi level in the source is less than a few thermal voltages (*kT)* below the valence band edge, the bandgap acts as an "energy filter", precluding tunneling from the exponential portion of the Fermi-Dirac distribution. If the gate bias is reduced sufficiently so that the bottom of the conduction band in the channel rises above the top of the valence band in the source, the tunneling abruptly shuts off. Due to this filtering of the Fermi-Dirac distribution function by the bandgap, the subthreshold slopes can be significantly less than 60 mV/decade.

A potential problem with tunneling transistors is that a very narrow bandgap semiconductor must be used to obtain sufficiently high ON current. However, narrow bandgap materials also lead to higher OFF currents, and are often incompatible with standard CMOS processing. To avoid this problem, a type-II hetero-junction tunneling transistor (HETT) can instead be employed. In such a case, the source-to-body contact has a staggered band lineup that creates an effective tunneling band gap, E_{geff}, which is smaller than that of the constituent materials. Such a band structure can also be realized in the Si/SiGe heterostructure material system, and complementary N- and P-HETTs can be fabricated, making this technology fully CMOS compatible. Figure 2 shows a schematic diagram of a complementary Si/SiGe HETT technology.

For the circuit simulations in this work, an optimized device structure was used. The simulated HETT devices have a gate length of 40 nm, and a high-k gate dielectric with effective gate oxide thickness of 1.2 nm. For NHETT, the source consists of pure Ge, with 3% biaxial compressive strain, and Si channel with 1% biaxial tensile strain. The complementary PHETT design includes a strained Si source and pure Ge channel. Using

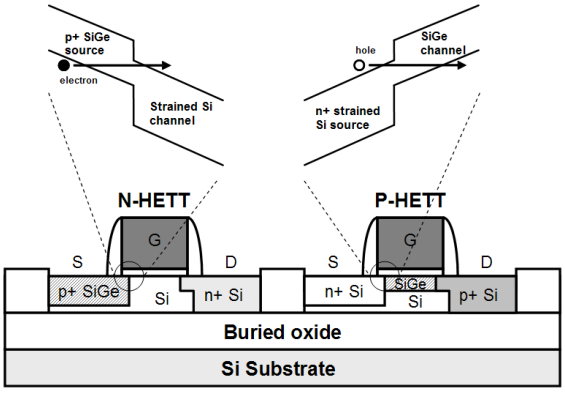


Figure 2. CMOS-compatible implementation of complementary tunneling FETs with type-II source-to-body hetero-junctions to improve device drive current.

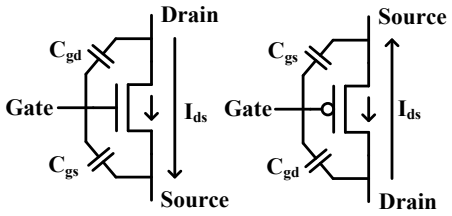


Figure 3. Device symbols for (a) NHETT (b) PHETT.

band offsets from [13], the effective bandgap for this structure is 0.22 eV. For the transport calculations, a non-local tunneling model [14] with a 2-band dispersion relationship within the gap was used. Effective masses are $0.17m_0$ near the conduction band and $0.105m_0$ near the valence band in the silicon channel, and $0.10m_0$ near the conduction band and $0.055m_0$ near the valence band in the pure Ge source [15]. The device has a 2nm gate overlap of the source and an abrupt source doping profile. A gate work function of ~4.4eV is used to set the OFF current to <1pA/μm.

3. HETT DEVICE MODELING

Since accurate analytical models for HETTs are not available, we first built a look-up table based model using Verilog-A to enable circuit simulations. This technique is a simple and accurate way of compact modeling for emerging devices [16] where analytical expressions for the I-V characteristics are not well established.

A look-up table model is built for I-V and C-V characteristics using T-CAD simulation data based on the device parameters described in the above section. The HETT is modeled as a three-terminal device (source, gate, and drain) and current is assumed to flow only between source and drain since gate leakage is negligible with high-k gate dielectrics. Two parasitic capacitors are modeled; C_{gd} and C_{gs}, which include inner fringing capacitance and overlap capacitance between gate and drain and between gate and source, respectively. Channel capacitance is negligible because the device has a fully-depleted channel and junction capacitance is also negligible due to its SOI-type substrate. As a result, we build three two-dimensional tables that are functions of two input voltages, V_{gs} and V_{ds}, for modeling HETTs: I_{ds} (V_{gs}, V_{ds}), C_{gd} (V_{gs}, V_{ds}), and C_{gs} (V_{gs}, V_{ds}). V_{gs} and V_{ds} are swept in 50mV steps in general, however in the slightly reverse biased region (-0.2V < V_{ds} < 0V) where I_{ds} transition is rapid V_{ds} steps are 10mV for the I_{ds} tables.

In Figure 3, new symbols for NHETT and PHETT are presented. An arrow inside the conventional MOSFET symbol denotes the direction of forward biased current, which is from drain to source for NHETT and vice versa for PHETT.

4. HETT-BASED CIRCUIT ANALYSIS

The steep subthreshold swing and larger ON current of HETTs compared to MOSFETs allow aggressive voltage scaling at iso-performance, enabling dynamic power reductions. To quantify this power reduction, ring oscillators are simulated with HETTs and compared with a commercial bulk CMOS 45nm technology. In addition, the circuit design impact of HETT limitations is also addressed in this section. HETT-based SRAM design is discussed in the Section 5.

4.1 Dynamic Power Reduction

A 31-stage ring oscillator with minimum sized inverters is used to evaluate dynamic power consumption. Leakage power is subtracted from total power to focus only on dynamic power in this section since the leakage power contribution was less than 10% (leakage is examined in more detail for SRAM in Section 5). In addition, minimum sized inverters are used since minimizing size results the least power for a given switching period.

Figure 4 shows the dynamic power reduction of the 31-stage ring oscillator with HETT devices compared to the commercial bulk CMOS 45nm technology. The CMOS technology has two types of logic devices: LP and GP. The LP devices are designed for low power operation and exhibit lower leakage than GP devices. Iso-speed dynamic power consumption of LP devices is expected to be worse because ON current in LP is smaller than in GP. With identical device sizes in both CMOS and

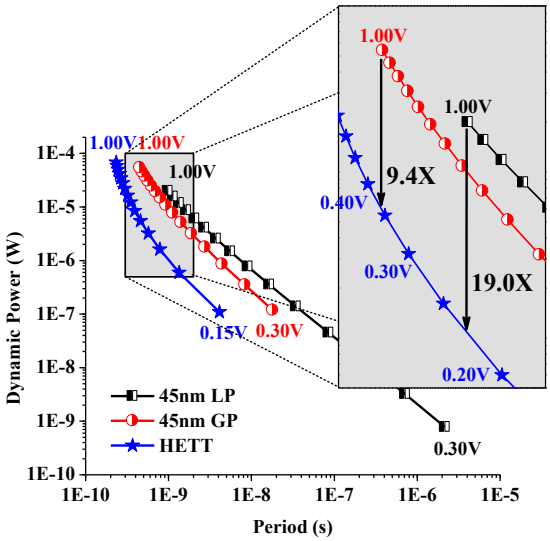
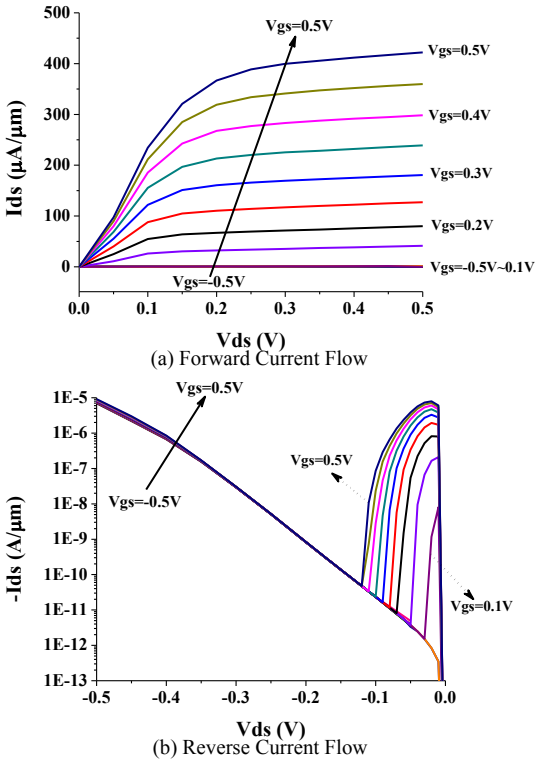


Figure 4. Comparison of dynamic power with commercial bulk-CMOS 45nm LP, 45nm GP, and HETT devices.

HETT technology, supply voltage is lowered from 1.0V to 0.3V in CMOS and from 1.0V to 0.15V in HETT with 0.05V steps. At 1.0V, the GP-based ring oscillator has a period of 450ps and 53.9µW dynamic power consumption. To maintain the same period, the ring oscillator with HETT consumes only 5.74µW at 0.355V, achieving a 9.4X dynamic power reduction. For 45nm LP, more dynamic power reduction is observed. At 1.0V, the LP ring oscillator period is 980ps and consumes 19.98µW while the HETT-based ring oscillator consumes 19X less power (1.05µW) at 0.226V with the same period.

4.2 Limitations of HETT-Based Circuits

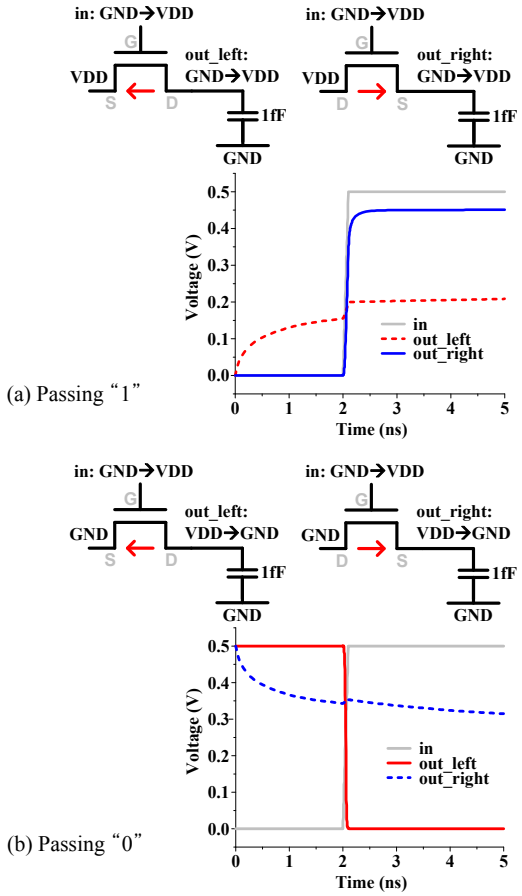
Asymmetric Current Flow



(a) Forward Current Flow

(b) Reverse Current Flow

Figure 5. (a) Forward bias and (b) reverse bias drain current of HETT device with L=40nm.



(a) Passing "1"

(b) Passing "0"

Figure 6. Two orientations (left and right) for implementing NHETT-based pass-gates passing a "1" (a) and passing "0" (b).

HETT source and drain are determined at fabrication time and current flow between the two nodes is not symmetric. Figure 5 demonstrates this asymmetric current flow in an NHETT. We assume that the nominal voltage of HETTs will be <0.5V as HETTs target ultra-low voltage applications and are well suited for this voltage regime. Figure 5(a) shows forward bias current with V_{gs} swept from 0V to 0.5V. The drain current curves look similar to CMOS devices. However, reverse bias current, where the voltage across the drain and source is negative, differs from CMOS devices as shown in Figure 5(b). Note that I_{ds} is negative in Figure 5(b). For most regions of V_{ds}, drain current is several orders of magnitude smaller than forward current. However, there are two cases where the reverse bias current becomes non-negligible. First is when V_{ds} is approximately –0.5V, at which point drain current become non-negligible regardless of V_{gs}. The second case occurs for positive V_{gs} combined with a small negative V_{ds}. PHETTs exhibit similar asymmetry in their current flow.

The asymmetric current flow does not restrict the use of traditional static CMOS logic circuits with pull-up network (PUN) and the pull-down network (PDN) because the current flow of each device in the PUN and PDN is uni-directional. However, pass-transistor and transmission-gate operation is limited since they require current flow in both directions. Figure 6 details the limitation of HETT-based pass-transistor circuits. Because the drain and source of the device are fixed, there are two ways to implement a pass-gate in a circuit: oriented left and right. In both cases, the current flow characteristics are classified again by two cases: passing logic "1" and passing logic "0".

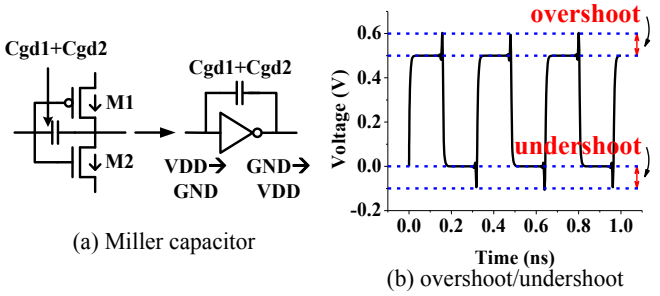
A pass-gate propagating logic "1" is shown in Figure 6(a), where left and right configurations are both illustrated. Before the input at the gate of pass-gate is switched at 2ns, the output of the rightward pass-gate stays near 0V while the output of leftward pass-gate is pulled up to ~150mV.

This is due to the fact that reverse OFF current can be larger than forward OFF current. When the input switches at 2ns, the output of the rightward pass-gate immediately switches to ~V_{DD} while the output of the leftward pass-gate remains near 200mV and increases very slowly. This clearly shows that forward ON current can strongly drive the output but reverse ON current cannot. For pass-gate passing logic "0" (Figure 6(b)), similar trends can be observed and only the leftward pass-gate functions well. This directional current driving capability renders pass-gate logic useless for HETT-based circuits. The asymmetric current flow also limits the use of the standard 6T SRAM cell and static latches/registers, which exploit pass-gates and transmission-gates as key components. Latches and registers can be implemented without pass-gates and transmission-gates by using clocked CMOS logic. An alternative SRAM cell topology will be discussed in Section 5.2.

Increased Miller Capacitance

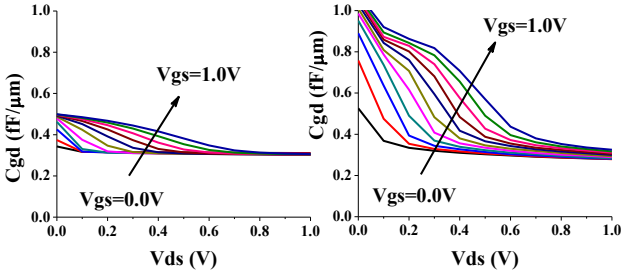
The capacitance between gate and drain is often referred to as the Miller capacitance as it is impacted as the Miller effect [17]. During a voltage transition, the two terminals of the Miller capacitor are moving in opposite directions such that the voltage change across the capacitor is twice the absolute voltage change (Figure 7(a)), hence this capacitance significantly impacts loading. In addition, it causes overshoots and undershoots during transitions due to capacitive coupling between input and output of the gate (Figure 7(b)), which results in additional capacitive loading, and performance overhead.

The Miller capacitance in HETTs is larger than the Miller capacitance in MOSFETs. This arises from the linking of the inversion layer in HETTs to the drain rather than the source, as is the case in MOSFETs. In HETTs with large gate bias, what can be viewed as a parasitic inversion layer forms with carriers drawn from the drain side – this inversion layer is not the primary form of current conduction in the device, hence the term parasitic. Under this bias condition, C_{gd} becomes essentially equivalent to the entire channel capacitance due to the parasitic inversion layer. This principle is the same as that described in detail in [18] for carbon nanotube-based tunneling FETs.



(a) Miller capacitor (b) overshoot/undershoot

Figure 7. (a) Miller capacitor acting as 2X larger capacitive loading and (b) overshoot and undershoot caused by capacitive coupling.



(a) CMOS (b) HETT

Figure 8. C_{gd} comparison of (a) CMOS (NMOS) and (b) HETT (NHETT).

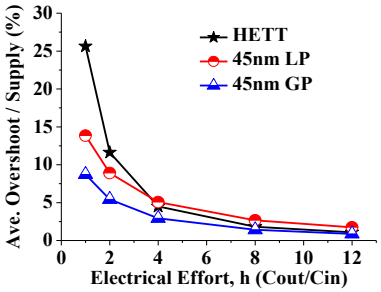


Figure 9. Overshoot effects in HETT are not significant with electrical effort of 4 or larger despite the larger Cgd.

In Figure 8, we find that the extracted C_{gd} of an NHETT is ~2X larger than C_{gd} of NMOS in a commercial bulk CMOS 45nm technology. To evaluate the impact of this larger Miller capacitance in HETTs, average overshoot and undershoot (as a percentage of the 0.5V supply) is evaluated and shown in Figure 9. If the electrical effort (from logical effort [19]) is larger than four, overshoot effects in HETTs are comparable to that in commercial 45nm CMOS technologies. Hence we conclude that for typical loads, the increased C_{gd} will not have significant impact on circuit performance, although it should be considered for very lightly loaded gates.

5. HETT-BASED SRAM DESIGN

The asymmetric current flow of HETT places restrictions on the use of pass-gate and transmission-gate. While this limitation is not severe for logic circuits, it poses a significant problem for the standard 6T SRAM, which uses pass gates for access transistors. In this section, we first analyze the implications of asymmetric current flow on SRAM operation and go on to propose an alternative 7T HETT-based SRAM cell topology. We then compare 7T performance and robustness to that of a CMOS-based 6T SRAM design.

5.1 Limitations in Standard 6T SRAM

CMOS Standard 6T SRAM

To understand the difference between HETT-based 6T SRAM and CMOS-based 6T SRAM, we trace current flow paths in read and write operations. Figure 10 shows a CMOS 6T SRAM cell storing "0". To read the stored value, bit lines (BIT, BIT_B) are pre-charged to V_{DD} and as word line (WL) is driven high, NPDL pulls down the voltage at BIT as shown in Figure 10(a). This pull down current or voltage can be sensed by a sense amplifier to determine the stored value. For writing a value "1", as shown in Figure 10(b), AXL pulls up internal node N0 while AXR pulls down internal node N1. However, since both access transistors are NMOS, which are better at pulling low, AXR plays the major role in write 1 operation. AXL aids in writing a 1 by pulling up N0 to a certain extent and making the bit flip more easily.

For this type of SRAM, read stability can be improved by increasing the sizing ratio of NPDL to AXL (or NPD to AX), which is commonly referred to as the cell β-ratio. As cell β-ratio increases, NPDL in Figure 10(a) holds the voltage at node N0 to ground more strongly during read, making it more stable. At the same time, this worsens writeability of the cell by making it more difficult to change the voltage at node N0. However as shown in Figure 10(b), since the pull down current path (AXR) plays the major role in writing, the size ratio of AXR to PPUR, or AX to PPU, is the critical one for writeability and can be improved by increasing this ratio. This implies that, up to a point, readability and writeability in CMOS 6T SRAM can be improved individually at the cost of larger area.

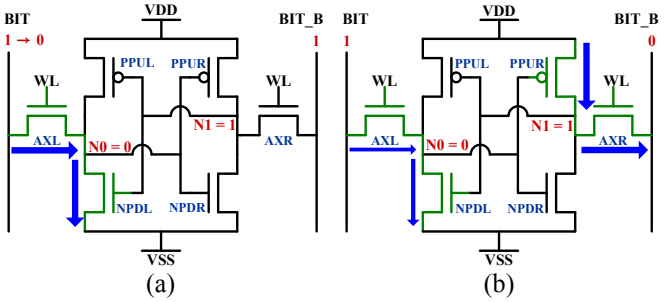


Figure 10. Current flow paths in (a) read and (b) write operations in CMOS 6T SRAM.

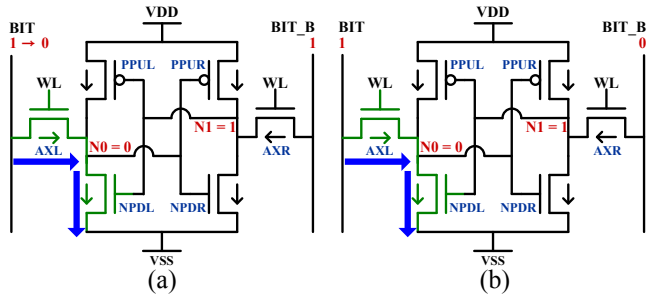


Figure 11. Current flow paths in (a) read and (b) write operations in HETT 6T SRAM with inward direction access transistors.

HETT Standard 6T SRAM with Inward Access Transistors

Due to its uni-directional nature, access transistors in HETT 6T SRAM can drive current either inward or outward only. Figure 11 shows a HETT 6T SRAM structure with inward current flow configuration and storing 0. Read operation for this SRAM is similar to a CMOS 6T SRAM. Bit-lines are precharged and current flows through AXL and NPDL. Therefore, similar to CMOS 6T SRAM, higher cell β-ratio is preferred for preventing read upset.

However, to write "1" to this cell, AXR cannot pull down the voltage at N1 since it can only conduct current inward, implying that AXL must pull up the voltage at N0 without differential aid, as shown in Figure 11(b). Therefore, the write operation is performed only by one side and the stronger current path is removed in HETT 6T SRAM. Since we are relying on an N-type transistor to drive the internal node voltage high, writeability of this cell is substantially worse than a CMOS 6T SRAM. To overcome poor writeability, AXL should be strengthened compared to NPDL, i.e., the cell β-ratio should be decreased. However, decreasing the cell β-ratio negatively affects the read margin.

This tradeoff between readability and writeability can be clearly seen if we plot static noise margin (SNM) of read and write operation versus cell β-ratio, as shown in Figure 12(a). SNM is the maximum DC voltage of the noise that can be tolerated by the SRAM and it is widely used for modeling stability of SRAM cells [20]. SNM can be defined for three

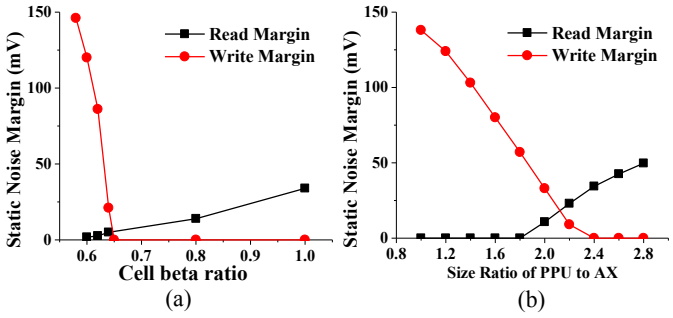


Figure 12. Static noise margins of HETT 6T SRAM with (a) inward and (b) outward access transistor with V_{DD}=0.5V.

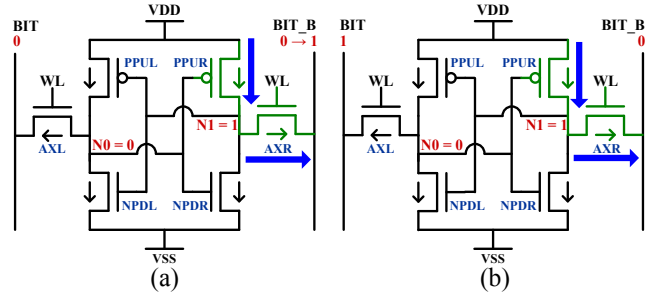


Figure 13. Current flow paths in (a) read and (b) write operations in HETT 6T SRAM with outward direction access transistors.

different operations – read, write, and standby (hold) – but only read and write margins are compared here since they limit SRAM stability. In SNM analysis for HETT-based SRAMs, all simulations use V_{DD} = 0.5V since HETTs are aimed at this voltage regime. For HETT 6T SRAM with inward access transistors with cell β-ratio of 1, read margin is 34mV but write margin is 0V, meaning that write operation is impossible. As we decrease the cell β-ratio to improve writeability, write margin becomes positive at a cell β-ratio of 0.64, however read margin at this point has degraded to <3 mV, indicating that the cell is highly vulnerable to read upset at this design point. From this we conclude that HETT 6T SRAM with inward access transistors is not feasible.

HETT Standard 6T SRAM with Outward Access Transistors

HETT 6T SRAM with outward access transistors has a similar limitation. Figure 13(a) shows a read operation, where bit lines (BIT BIT_B) are pre-discharged and BIT_B is charged through AXR and must be sensed. For writing, AXR must drive internal node N1 to ground and flip the stored value without differential assistance from AXL. Since both of these operations involve PPUR and AXR, adjusting the ratio of PPUR to AXR strengths will improve one operation and worsen the other. This tradeoff can be clearly seen in Figure 12(b). The read operation requires PPUR to AXR ratio higher than 1.8, while the write operation malfunctions when the ratio is higher than 2.4. In the remaining design space the SNM for read/write operations is limited to <50 mV, which is insufficient. Therefore, an alternative SRAM topology is needed to achieve robust low leakage SRAM with HETTs.

5.2 7T SRAM for HETT

Figure 14 shows the proposed 7T SRAM structure that overcomes readability/writeability tradeoffs in HETT-based 6T SRAM. The basic structure is based on HETT 6T SRAM with outward access transistors, but includes an additional NHETT labeled "NRD" that is used to read out the cell contents.

Unlike the other 6T SRAM structures, read operation in 7T SRAM is conducted solely through NRD. Figure 15 illustrates how NRD in each cell is connected in the array structure. The source of NRD is connected to

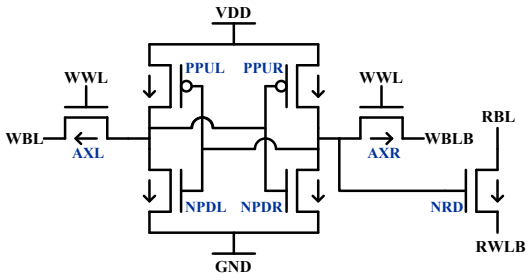


Figure 14. Proposed HETT 7T SRAM structure.

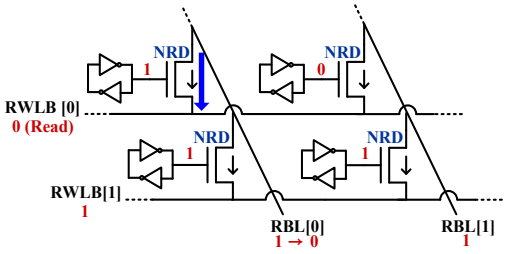


Figure 15. Read operation in 7T SRAM array.

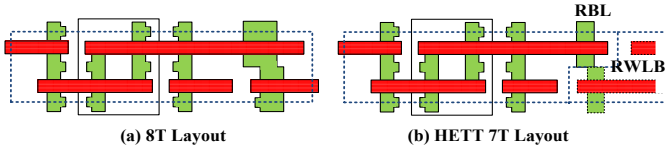


Figure 16. (a) 8T layout [22] and (b) corresponding HETT 7T layout.

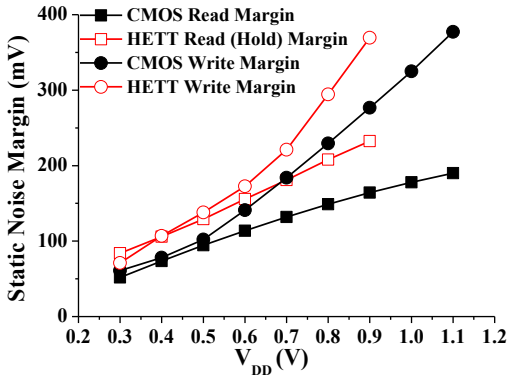


Figure 17. Read/Write margin of 45nm commercial bulk CMOS 6T SRAM and HETT 7T SRAM.

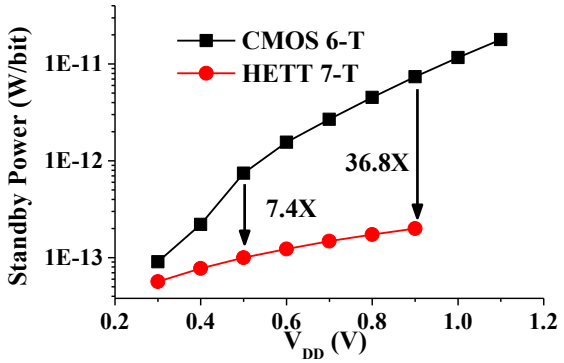


Figure 18. Standby power of CMOS 6T and HETT 7T SRAM.

that of other cells in the same word (RWLB), while the drain is connected to that of other cells in same column (RBL). To read values in word[0] (top row of Figure 15), bit-lines (RBL[0], RBL[1]) are precharged and RWLB[0] is asserted (driven to ground) while all other RWLBs are set to V_{DD}. Since the source of the NRDs in word[0] are set to ground, cells that store value '1' can discharge the bit line, as depicted with the thick arrow in Figure 15. With CMOS transistors, this read scheme does not work because, as RBL[0] is discharged, other cells storing '1' on the same bit line can start charging up RBL[0] as in the case of the bottom-left cell in Figure 15. However, by leveraging the asymmetric nature of HETTs, this unwanted reverse-direction charging current is eliminated without the cost of an additional transistor, as in the well-known 8T structures [21]. The HETT 7T SRAM is estimated to have <15% area overhead over a standard 6T while 8T SRAM exhibits 29% cell area overhead [22]. Figure 16 shows that two read transistors (NRD in Figure 14) from adjacent cells can be abutted in 7T SRAM, making the overhead for two 7T cells equal to that of one 8T cell. Moreover, as will be shown below the 7T cell with all transistors at minimum size shows improved robustness over 6T at low voltage, hence if an upsized 6T were used to achieve iso-robustness the area penalty would be much smaller than 15%.

A write operation in this 7T structure is equivalent to the HETT 6T SRAM with outward access transistors. However, since the read/write operations are performed by separate current paths, device sizes for all transistors other than NRD can be chosen to favor writeability. The outward access transistor scheme is used for its superior writeability over the inward configuration when all transistors are of near-minimum width to improve density.

We compare SNM of HETT-based 7T SRAM to a 45nm commercial bulk CMOS 6T SRAM cell provided by a foundry. All HETT devices are set to equal (minimum) width for maximum density. Read and write margins of both types of SRAMs across a range of supply voltages are plotted in Figure 17. SNM for HETT is analyzed with supply voltages up to 0.9V only since HETT is designed for low voltage (~0.5V) operation. Write margins of HETT 7T SRAM are more than 30% higher than CMOS 6T SRAM for supply voltages of >0.4V as shown in Figure 17.

Since the read operation uses an additional read transistor in the HETT 7T SRAM and all other transistors are in standby (hold) state during read operation, hold margin is equivalent to read margin in HETT 7T SRAM. Given this, HETT 7T read margin is 232 mV at V_{DD}=0.9V and 129 mV at 0.5V, which is 41% and 37% higher than commercial bulk CMOS 6T SRAM, respectively. Such improvements in read/write margin can be observed for V_{DD} down to 0.3V, suggesting that improved read/write robustness can be achieved with HETT 7T SRAM over traditional CMOS at low voltage.

Finally, HETT-based SRAM standby power is significantly reduced compared to CMOS 6T SRAM, as seen in Figure 18. At a supply voltage of 0.9V, standby power is reduced by 36.8X and at 0.5V, by 7.4X. This clearly shows the promising low-leakage properties of HETT devices for future memory-dominated low-power applications.

6. CONCLUSIONS

A circuit perspective of a new promising tunneling transistor, HETT, with steep subthreshold swing for extremely low power applications was presented in this paper. We observed 9−19X dynamic power reduction with HETT-based circuits due to their improved voltage scalability. We examined the limitations of HETTs as they relate to circuit operation. To overcome and exploit the inherent device asymmetry, a new HETT-based SRAM cell topology was presented with 7−37X leakage power reduction.

7. ACKNOWLEDGMENTS

This work was supported by the DARPA STEEP program, under AFRL contract #FA8650-08-C-7806.

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